CLAIMS

1. A method comprising:

receiving a first digital control value indicating the phase of a first clock signal;

receiving a second digital control value indicating the phase of a second clock signal; and

comparing the first and second digital control values to detect a phase relationship between the first and second clock signals.

2. A method as recited in claim 1, wherein the phase relationship between the first and second clock signals varies with PVT variations, the method further comprising adjusting a PVT-sensitive circuit as a function of the detected a phase relationship between the first and second clock signals.

3. A method as recited in claim 1, further comprising:

calibrating the phase of the first clock signal relative to a received data signal;

clocking an input latch with the first clock signal to latch the received data signal and to produce a captured data signal; and

latching the captured data signal at a time that varies as a function of the detected phase relationship between the first and second clock signals to produce a captured data signal.

4. A method as recited in claim 1, further comprising:

calibrating the phase of the second clock signal relative to a received third clock signal;

identifying the phase of the third clock signal relative to the first clock signal with reference to the detected phase relationship between the first and second clock signals.

5. A method as recited in claim 1, wherein the phase of the second clock signal is established by setting the value of the second digital control value; the method further comprising:

comparing the first and second clock signals in a calibration procedure while varying the second control value to produce a predetermined phase relationship between the first and second clock signals;

deriving a correction value from the second digital control value that produces the predetermined phase relationship between the first and second clock signals; and

subsequent to the calibration procedure, compensating the second digital control value with the derived correction value to account for different propagation delays of the first and second clock signals.

6. A device comprising:

a first clock generator that generates a first clock signal in response to a first digital control value, wherein the first digital control value establishes the phase of the first clock signal;

a second clock generator that generates a second clock signal in response to a second digital control value, wherein the second digital control value establishes the phase of the second clock signal;

phase detection logic that compares the first and second digital control values to detect a phase relationship between the first and second clock signals.

7. A device as recited in claim 6, further comprising a PVT-sensitive circuit that is responsive to the phase detection logic to compensate for PVT variations.

8. A device as recited in claim 6, further comprising:

calibration logic that sets the first digital control value to calibrate the phase of the first clock signal relative to a received data signal;

an input latch that is clocked by the first clock signal to latch the received data signal and to produce a captured data signal; and

latching logic that is responsive to the phase detection logic to latch the captured data signal to produce a synchronized data signal relative to the second clock signal.

9. A device as recited in claim 6, further comprising:

calibration logic that receives a third clock signal having an undetermined phase relative to the first clock signal and that sets the second digital control value to calibrate the phase of the second clock signal relative to the third clock signal;

wherein the phase detection logic compares the first and second digital control values to determine the phase of the third clock signal relative to the first clock signal.

10. A device as recited in claim 6, further comprising:

calibration logic that operates in a calibration procedure to compare the first and second clock signals while varying at least one of the first and second digital control values to produce a predetermined phase relationship between the first and second clock signals;

wherein the phase detection logic derives at least one correction value from said at least one of the first and second digital control values that produce the predetermined phase relationship; and

wherein the calibration logic compensates at least one of the first and second digital control values with the at least one derived correction value to account for different propagation delays of the first and second clock signals.

11. A method of phase detection, comprising:

receiving a clock signal that has an undetermined phase relative to a reference clock signal;

generating a measurement clock signal having a phase that is established relative to the reference clock signal by a phase control value;

setting the phase control value to produce a predetermined phase relationship between the measurement clock signal and the received clock signal; and

evaluating the set phase control value to detect a measured phase relationship of the received clock signal relative to the reference clock signal.

12. A method as recited in claim 11, wherein setting the phase control value comprises varying the phase control value until the phase of the measurement clock signal is approximately equal to the phase of the received clock signal.

13. A phase detection device, comprising:

a clock generator that generates a measurement clock signal having a phase that is established relative to a reference clock signal by a phase control value;

calibration logic that varies the phase control value to produce a predetermined phase relationship between the measurement clock signal and a received clock signal that has an undetermined phase;

evaluation logic that evaluates the phase control value to detect a phase relationship between the received clock signal and the reference clock signal.

14. A phase detection device as recited in claim 13, wherein the calibration logic varies the phase control value until the phase of the measurement clock signal is approximately equal to the phase of the reference clock signal.

15. A method comprising:

generating a plurality of clock signals in response to digital control values that specify desired relative phases of the clock signals, the clock signals being subject to different propagation delays;

varying the digital control values in a calibration procedure to produce a predetermined phase relationship between the clock signals;

deriving correction values from the digital control values that produce the predetermined phase relationship;

subsequent to the calibration procedure, setting the digital control values to produce desired clock signal phases; and

compensating the digital control values with the derived correction values to account for the different propagation delays of the clock signals.

16. A method as recited in claim 15, wherein the clock signals have approximately identical phases when in the predetermined phase relationship.

17. A method as recited in claim 15, wherein generating the clock signals comprises deriving the clock signals from one or more common reference clock signals.

18. A device comprising:

a plurality of clock generators that generate respective clock signals in response to digital control values that specify desired relative phases of the clock signals, the clock signals being subject to different propagation delays;

calibration logic that varies the digital control values in a calibration procedure to produce a predetermined phase relationship between the clock signals;

wherein the calibration logic derives one or more correction values from the digital control values that produce the predetermined phase relationship, said

correction values being used subsequent to the calibration procedure to account for the different propagation delays of the clock signals.

19. A device as recited in claim 18, wherein the clock signals have approximately identical phases when in the predetermined phase relationship.

20. A device as recited in claim 18, wherein the clock generators generate the clock signals from one or more common reference clock signals.

21. A method of phase detection, comprising:

generating a measurement clock signal having a phase that is established relative to a reference clock signal by a phase control value;

delaying the measurement clock signal by a phase delay that varies with PVT variations;

varying the phase control value to find a PVT adjustment value that produces a predetermined phase relationship between the delayed measurement clock signal and the reference clock signal;

adjusting a PVT-sensitive circuit as a function of the PVT adjustment value to compensate for PVT variations in the PVT-sensitive circuit.

22. A method as recited in claim 21, wherein varying the phase control value comprises varying the phase control value until the phase of the measurement clock signal is approximately equal to the phase of the reference clock signal.

23. A device comprising:

a clock generator that generate a measurement clock signal having a phase that is established relative to a reference clock signal by a phase control value;

one or more delay elements configured to delay the measurement clock signal by a phase delay that varies with PVT variations;

calibration logic that varies the phase control value to find a PVT adjustment value that produces a predetermined phase relationship between the delayed measurement clock signal and the reference clock signal;

a PVT-sensitive circuit that is responsive to the PVT adjustment value to compensate for PVT variations in the PVT-sensitive circuit.

24. A device as recited in claim 21, wherein the calibration logic varies the phase control value until the phase of the measurement clock signal is approximately equal to the phase of the reference clock signal.

25. A method of synchronizing a received data signal with a target timing signal, comprising:

generating an input timing signal having a phase that is established relative to the target timing signal by a input phase control value;

setting the input phase control value to calibrate the phase of the input timing signal relative to the received data signal;

clocking the received data signal with the generated input timing signal to produce a captured data signal;

evaluating the input phase control value to determine an appropriate timing phase at which to clock the captured data signal for synchronization with the target timing signal; and

clocking the captured data signal at the determined appropriate timing phase to produce a synchronized data signal relative to the target timing signal.

26. A method as recited in claim 25, wherein the evaluating comprises comparing the input phase control value to a reference value.

27. A method as recited in claim 25, wherein:

the evaluating comprises comparing the input phase control value to a reference value; and

the reference value represents a 90° phase offset from the target timing signal.

28. A method as recited in claim 25, wherein the evaluating comprises comparing the input phase control value to a target phase control value that establishes the phase of the target timing signal.

29. A method as recited in claim 25, further comprising:

generating the target timing signal in response to a target phase control value that establishes the phase of the target timing signal.

30. A method as recited in claim 25, further comprising:

generating the target timing signal in response to a target phase control value that establishes the phase of the target timing signal; and

wherein the evaluating comprises comparing the input phase control value to the target phase control value.

31. A method as recited in claim 25, wherein the input phase control value is a digital word.

32. A method as recited in claim 25, wherein the evaluating determines the appropriate timing phase to be (a) the phase of the target timing signal if the evaluation indicates that the target timing signal lags the input timing signal by more than 90° or (b) a phase that is 180° relative to the phase of the target timing signal if the evaluation indicates that the target timing signal lags the input timing signal by less than 90°.

33. A method as recited in claim 25, further comprising:

clocking the synchronized data signal with the target timing signal.

34. A method of synchronizing a received data signal with a target clock signal, comprising:

setting a target phase control value to establish the phase of the target clock signal;

setting an input phase control value to establish the phase of an input clock signal;

clocking the received data signal with the input clock signal to produce a captured data signal;

comparing the target phase control value and the input phase control value to determine an appropriate timing phase at which to clock the captured data signal for synchronization with the target clock signal; and

clocking the captured data signal at the determined appropriate timing phase to produce a synchronized data signal relative to the target clock signal.

35. A method as recited in claim 34, wherein the comparing comprises detecting whether the target clock signal lags the input clock signal by a predetermined amount based on the target and input phase control values.

36. A method as recited in claim 34, wherein the comparing comprises detecting whether the target clock signal lags the input clock signal by 90° based on the target and input phase control values.

37. A method as recited in claim 34, wherein the phase control values are digital words.

38. A method as recited in claim 34, wherein the comparing determines the appropriate timing phase to be (a) the phase of the target clock signal if the comparing indicates that the target clock signal lags the input timing signal by more than 90° or (b) a phase that is 180° relative to the phase of the target clock signal if the comparing indicates that the target clock signal lags the input clock signal by less than 90°.

39. A method as recited in claim 34, further comprising:

clocking the synchronized data signal with the target timing signal.

40. A method as recited in claim 34, further comprising:

setting the input phase control value to calibrate the phase of the input clock signal relative to the received data signal.

41. A device for synchronizing a received data signal with a target clock signal, comprising:

an input clock generator that generates an input clock signal at a calibrated phase relative to the received data signal, wherein the input clock generator receives an input phase control value that establishes the calibrated phase of the input clock signal;

an input latch that is clocked by the input clock signal to latch the received data signal and to produce a captured data signal;

evaluation logic that evaluates the input phase control value to determine an appropriate timing phase at which to clock the captured data signal for synchronization with the target clock signal; and

latching logic configured to latch the captured data signal at the determined appropriate timing phase to produce a synchronized data signal relative to the target clock signal.

42. A device as recited in claim 41, further comprising:

a target clock generator that generates the target clock signal, wherein the target clock generator receives a target phase control value that establishes the phase of the target clock signal;

wherein the evaluation logic compares the target phase control value and the input phase control value to determine the appropriate timing phase.

43. A device as recited in claim 41, wherein the evaluation logic compares the input phase control value to a reference value.

44. A device as recited in claim 41, wherein:

the evaluation logic compares the input phase control value to a reference value; and

the reference value represents a 90° phase difference from the target timing signal.

45. A device as recited in claim 41, wherein the input phase control value is a digital word.

46. A device as recited in claim 41, wherein the evaluation logic determines the appropriate timing phase to be (a) the phase of the target clock signal if the target clock signal lags the input clock signal by more than 90° or (b) a phase that is 180° relative to the phase of the target clock signal if the target clock signal lags the input clock signal by less than 90°.

47. A device as recited in claim 41, further comprising:

a second input latch that clocks the synchronized data signal in response to the target timing signal.